

OPTIMIZED FLASH MEMORY CELL

ABSTRACT

A flash memory comprising floating gate devices being connected to one-another through their source electrodes being self-aligned to their respective gate electrodes, a local tungsten interconnect making a substantially continuous connection to the sources. The flash memory is formed by forming floating gate devices, each comprising a floating gate, forming a source electrode for each floating gate device and connecting each source electrode together by a conductive implant into a defined active area, forming a nitride barrier layer overlying each transistor gate, forming a planarized insulation layer over the nitride barrier layer, removing portions of the planarized insulation layer while using the nitride barrier layer to self-align an interconnect via opening to the source electrodes, forming a metal interconnect into the interconnect via, the metal interconnect running a major length of the interconnected source electrodes and making contact therebetween, and forming a metal drain plug for each floating gate device.